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				Application Number		10/624 728
				Filing Date		
				First Named Inventor		Leo Mathew
				Group Art Unit		2825
Examiner Name		Siek, V.				
Sheet	1	of	1	Attorney Docket Number		SC12862TC

U. S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. *	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No. *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
VS	AA	Geppert, "Momentum Builds for Multiple-Gate Transistors," IEEE, Spectrum, pp. 1-3 (2003).
VS	AB	Ohr, "FinFETs and InP lcs Vie for Dominance in Future lcs," Silicon Strategies, pp. 1-4 (2003).
VS	AC	Nowak et al., "A Functional FinFET-DGCMOS SRAM Cell," IEEE, 4 pgs., (2002).
VS	AD	Copy of related patent application 10/074,732.
Examiner Signature	YUTHE SIEK	
Date Considered	7/15/05	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

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